

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:)
BERTRAND ET AL.) Examiner: Anh Q. TRA
)
Serial No. 10/813,564) Art Unit: 2816
)
Filing Date: MARCH 30, 2004) Docket No.:
) 54500
For: TWO-THRESHOLD COMPARATOR)
INSENSITIVE TO ITS ENVIRONMENT)
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PRE-APPEAL BRIEF REQUEST FOR REVIEW

MS AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Responsive to the final Official Action of August 13, 2007, and in connection with the Notice of Appeal filed concurrently herewith, please consider the remarks set out below.

REMARKS

Based upon the arguments presented below, Applicants respectfully request the Pre-Appeal Conference Panel reconsider and withdraw the Examiner's rejections of the claims.

I. The Claimed Invention

Independent Claim 12 is directed to a comparator with two thresholds comprising a two-threshold latch including an input and an output respectively forming an input and an output of the comparator, and including a first node between a first power supply terminal and the output of the comparator. The comparator further includes a first negative feedback loop acting on the first node for setting a first threshold of the comparator as a function of a first

power supply potential applied to the first power supply terminal, and as a function of a first reference potential.

The first threshold is a voltage rise triggering threshold, and the first reference potential is less than or equal to the first power supply potential, which is positive. The difference between the first power supply potential and the first reference potential is positive and increases as a function of the first power supply potential to limit an increase in the first threshold when the first power supply potential increases.

Independent Claim 23 is directed to a comparator similar to independent Claim 12 and further recites a latch connected between first and second power supply terminals and having a voltage rise triggering threshold and a voltage drop triggering threshold, a second node between the second power supply terminal and the output of the comparator, and a second negative feedback loop for setting a second threshold of the comparator as a function of a second power supply potential applied to the second power supply terminal, and as a function of a second reference potential applied to said second negative feedback loop. Independent Claim 33 is directed to a method counterpart of independent Claim 23.

II. The Claims Are Patentable

The Examiner has rejected independent Claims 12, 23, and 33 over the Naura patent, assigned to the present application's assignee. Naura discloses a threshold amplifier where the transistors that set voltage rise threshold and voltage drop threshold in the amplifier are controlled by respective bias control circuits. (Col. 4, lines 23-27). Naura discloses the threshold amplifier 2 including an inverter stage 2a, and a stage 2b for setting the voltage rise threshold and the voltage drop threshold. (Col. 3, lines 15-17). Further, Naura further discloses that the transistors T6 and T5 set the voltage rise threshold and voltage drop threshold, respectively. (Col.3, lines 39-42 & 55-57). Naura discloses that the first bias control circuit CP1 and the second bias control circuit CP2 are associated with transistors T5 and T6, respectively.

(Col. 4, lines 22-27). More simply, control circuit CP1 [T7-8] controls the voltage drop threshold, and control circuit CP2 [T9-10] controls the voltage rise threshold. (See Figure 5).

The Examiner contended that the trio of transistors T5, T7, T8 (T7, T8 being part of control circuit CP1, which controls the **voltage drop threshold**), controlling "output pull up threshold at node C", discloses the first negative feedback loop acting on the first node for setting the voltage rise triggering threshold of the comparator, as in the claimed invention.

Applicants submit that the Examiner has mischaracterized Naura. The cited trio of transistors, noted as circuit CP1 in Naura, expressly sets the voltage drop threshold of the amplifier of Naura. (Col. 3, lines 37-52 & Col. 4, lines 23-27). Indeed, Naura recites "[i]n practice, when the output S of the inverter stage is at zero, the transistor T5 dictates a minimum voltage in the range of the threshold voltage of a P type transistor V_{tp} on the node C." (Col. 3, lines 43-47). The Examiner also contended that the present application fails to support the voltage rise triggering threshold of the claimed invention, and from this, contended that any voltage rise threshold meets the claimed feature. For the convenience of the Panel and the Examiner, Applicants have reproduced the relevant portion of the present application.

[0001] The invention relates generally to a comparator with two switching thresholds. Such a device is commonly called a hysteresis trigger, and hereinafter in this document, it shall simply be called a trigger.

[0002] Such a trigger provides an output signal OUT at the output indicating the logic value of an analog input signal IN. The signal OUT is equal to the power supply potential VDD (corresponding to a logic one) when the signal IN rises to an upper threshold V_H, and the signal OUT is equal to zero when the signal IN descends to a lower threshold V_B (Figure 1). ***

[0004] More specifically, the present invention relates to a comparator with two thresholds V_H, V_B comprising a latch with two switching thresholds.
(Paragraphs 1-2, & 4; Emphasis added).

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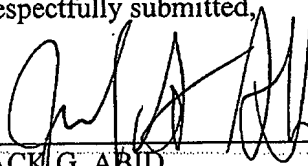
Indeed, Applicants have amended the claims more than once and filed a Request for Continued Examination in an attempt to satisfy the Examiner. Applicants now submit for a third time to the U.S. Patent & Trademark Office that a person of ordinary skill in the art would appreciate a clear and unambiguous meaning for the claim recitation of the voltage rise triggering threshold of the comparator. Accordingly, since Naura fails to disclose the first negative feedback loop acting on the first node for setting the voltage rise triggering threshold of the comparator, as in the claimed invention, for this reason alone, independent Claims 12, 23, and 33 are patentable.

Furthermore, the Examiner contended that Naura discloses the first reference potential [Examiner cites Vref1, see Final Official Action Page 2, line 18] is less than or equal to the first power supply potential [Examiner cites Vdd or ground, see Final Official Action Page 2, line 17], as recited in the independent claims. The Examiner correctly notes that Vref1 of Naura is equal to "about 1 volt." (Col. 5, line 35). Applying the Examiner's own rejection formulation to the required relationships of the claimed invention, Applicants respectfully point out that Vref1 (1 volt, a positive value) of Naura cannot be less than or equal to GND ground-zero potential (0 volts) of Naura nor be positive, relationships recited within the independent claims, helpfully bracketed above.

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Accordingly, for all the reasons above, independent Claims 12, 23, and 33 are patentable over the prior art. Their respective dependent claims, which recite yet further distinguishing features, are also patentable over the prior art and require no further discussion herein.

Respectfully submitted,



JACK G. ABID
Reg. No. 58,237
Allen, Dyer, Doppelt, Milbrath
& Gilchrist, P.A.
255 S. Orange Avenue, Suite 1401
Orlando, Florida 32802
407-841-2330
Attorney for Applicants